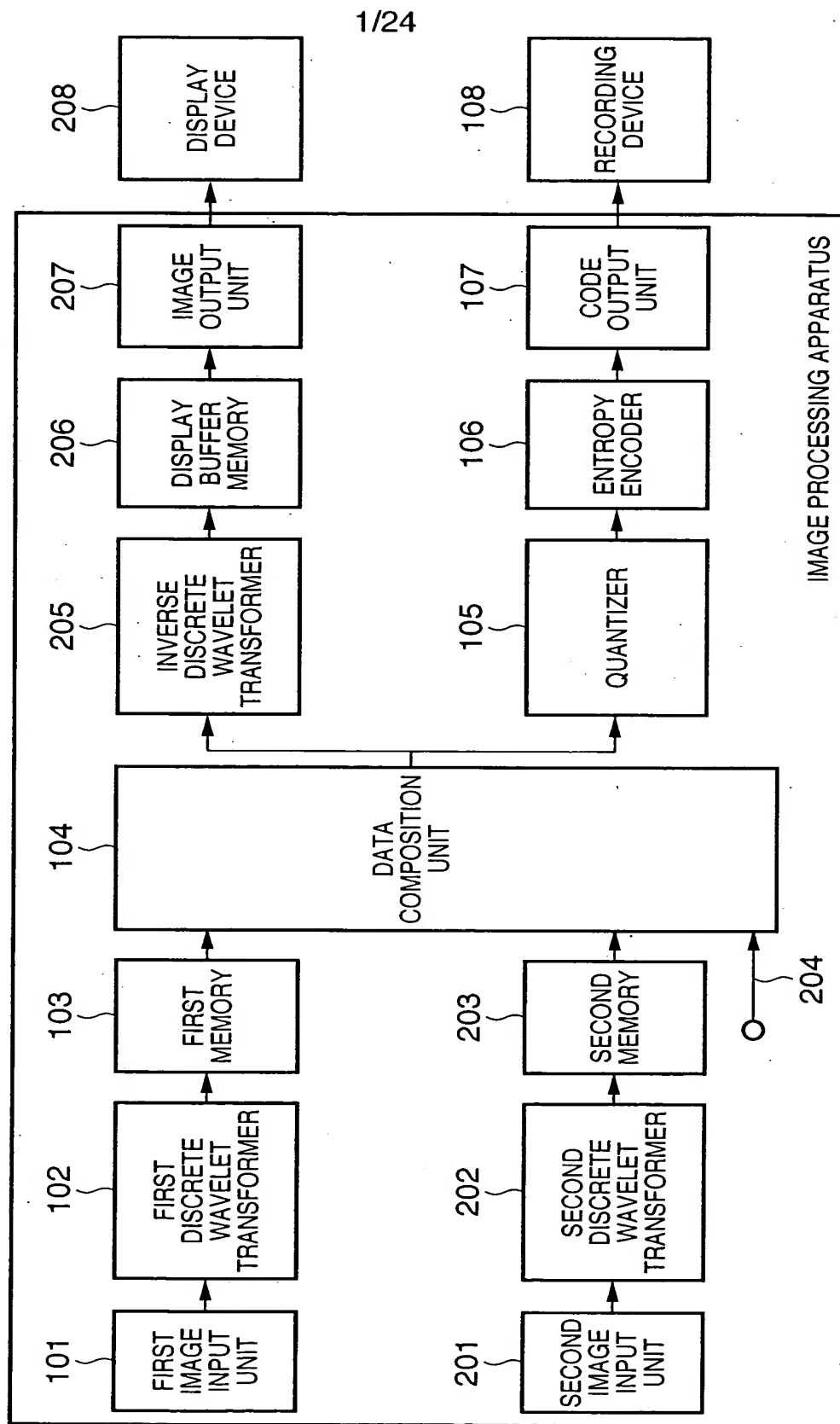


FIG. 1



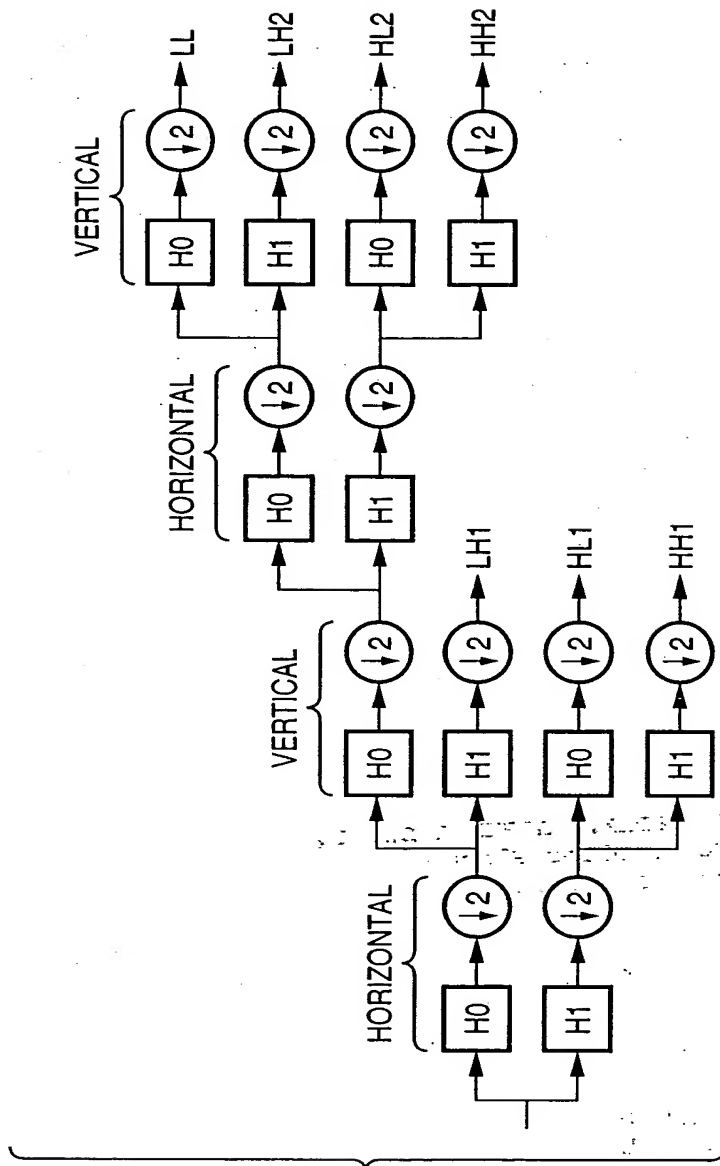


FIG. 2A

LL	HL2	HL1	
LH2	HH2		HH1
		LH1	

FIG. 2B

FIG. 3

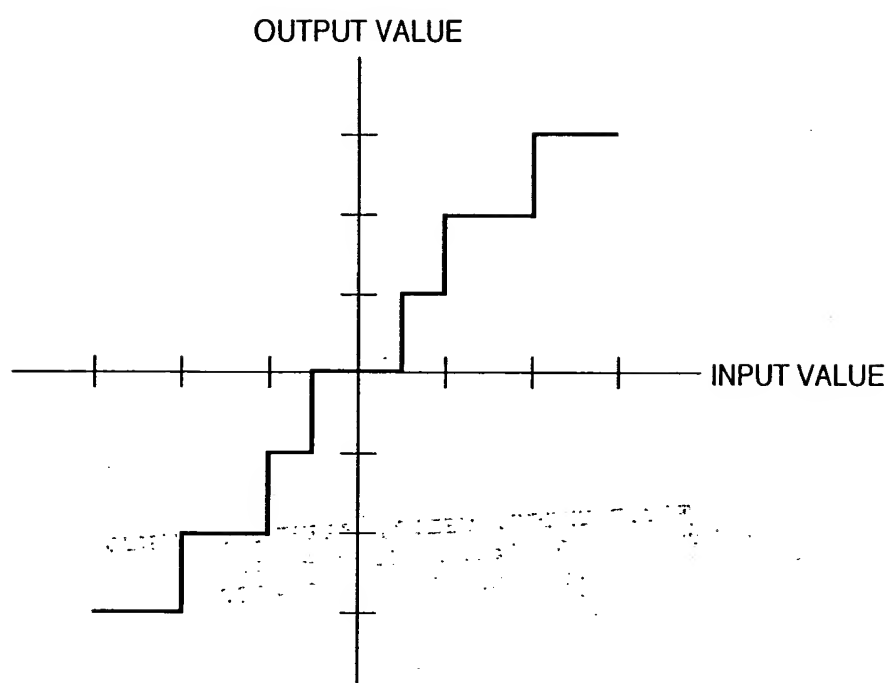


FIG. 4

FIG. 4 is a schematic diagram of a system for processing data. The system includes a data source 100, a processor 110, and a display 120. The data source 100 is connected to the processor 110, which is connected to the display 120. The processor 110 is configured to receive data from the data source 100, process the data, and output the processed data to the display 120. The display 120 is configured to display the processed data to a user.

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FIG. 5A

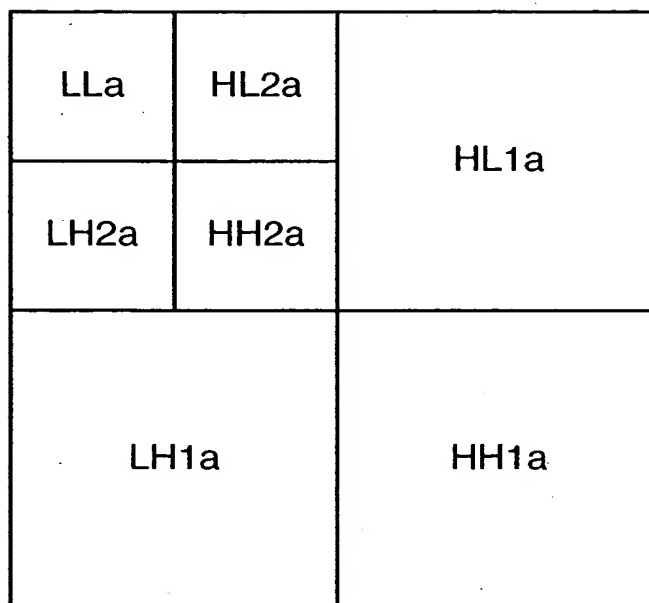


FIG. 5B

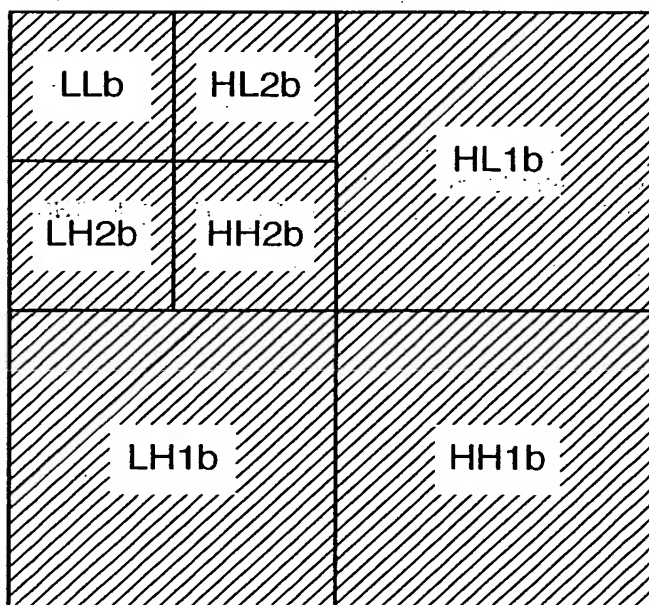
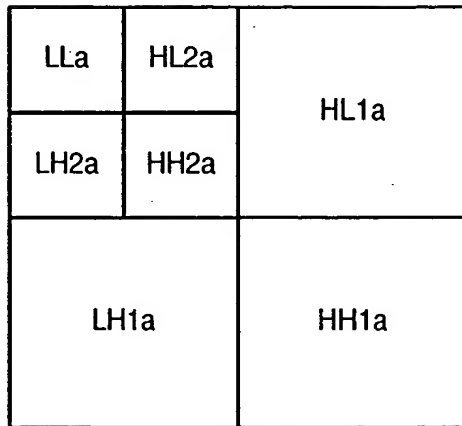
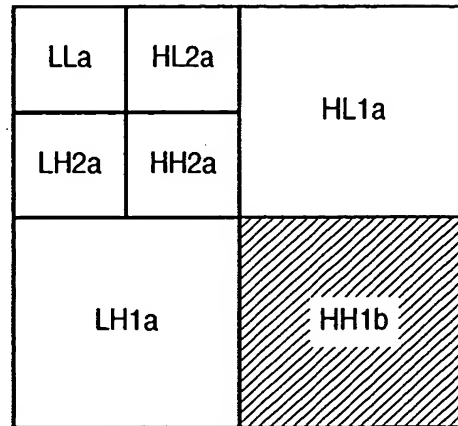
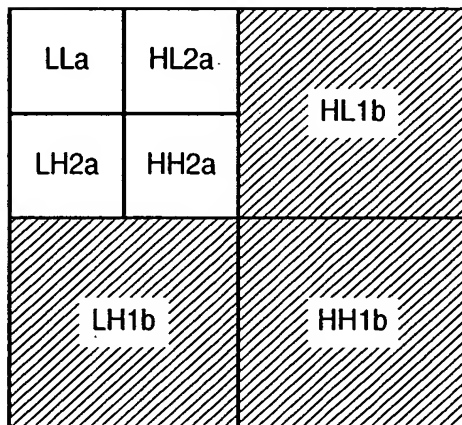


FIG. 6A

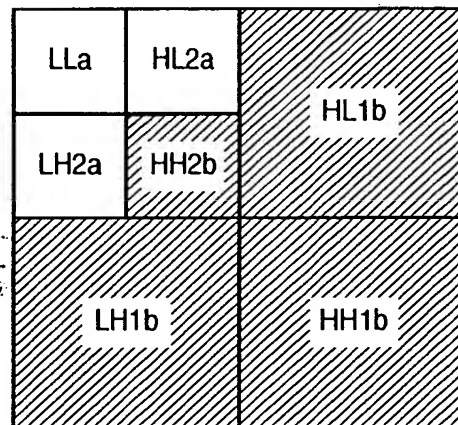
START OF SWITCHING

FIG. 6B

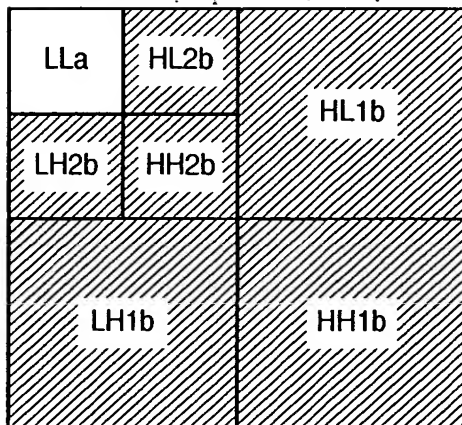
1ST TO 30TH FRAMES

FIG. 6C

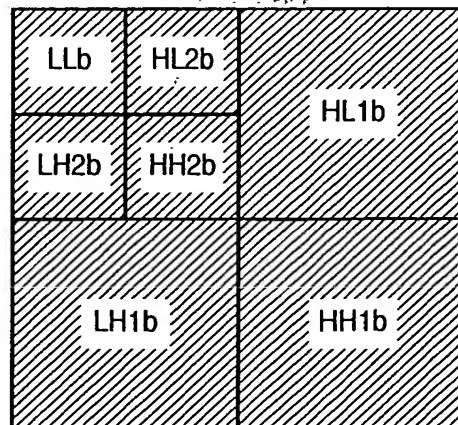
31ST TO 60TH FRAMES

FIG. 6D

61ST TO 90TH FRAMES

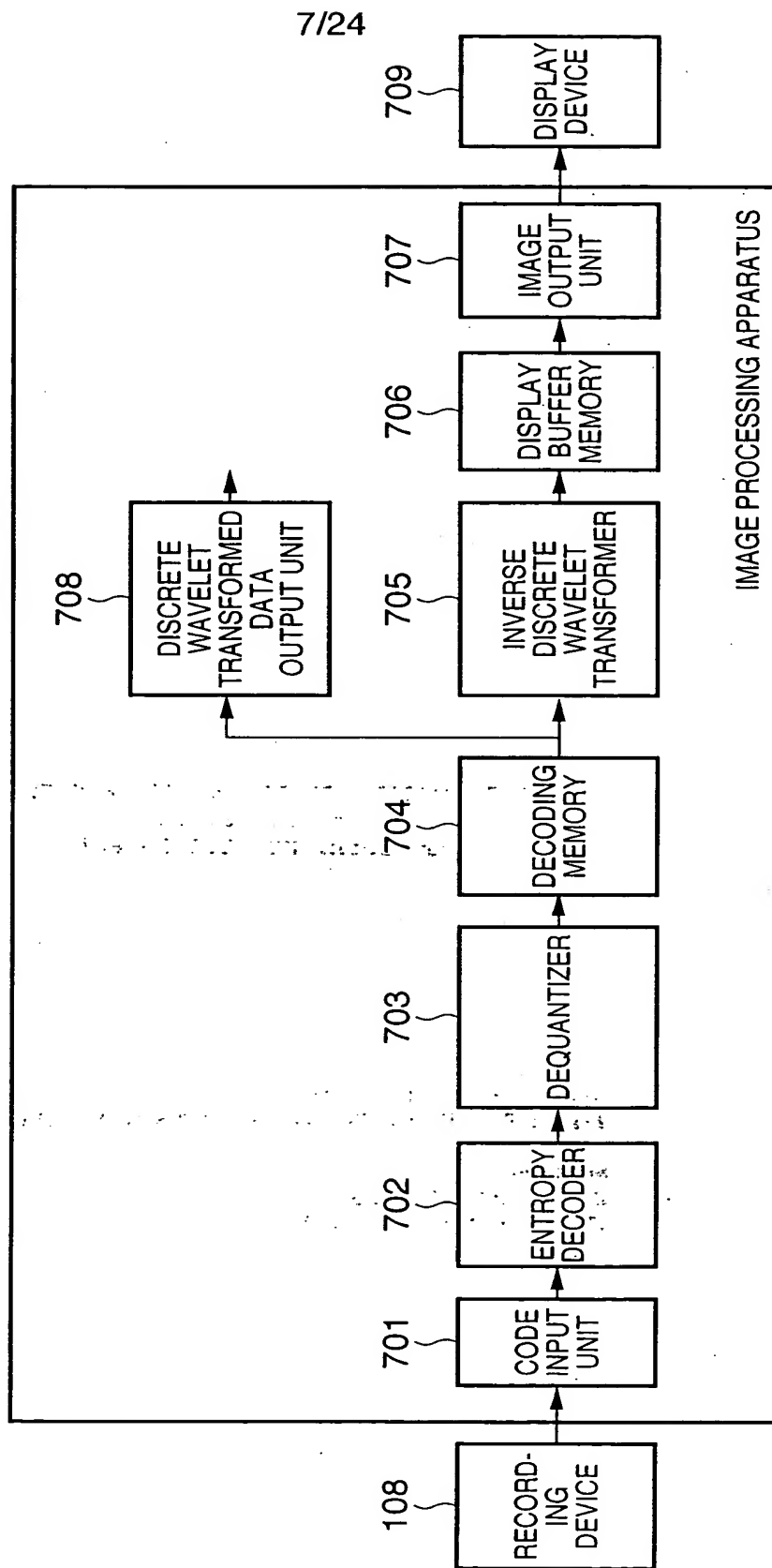
FIG. 6E

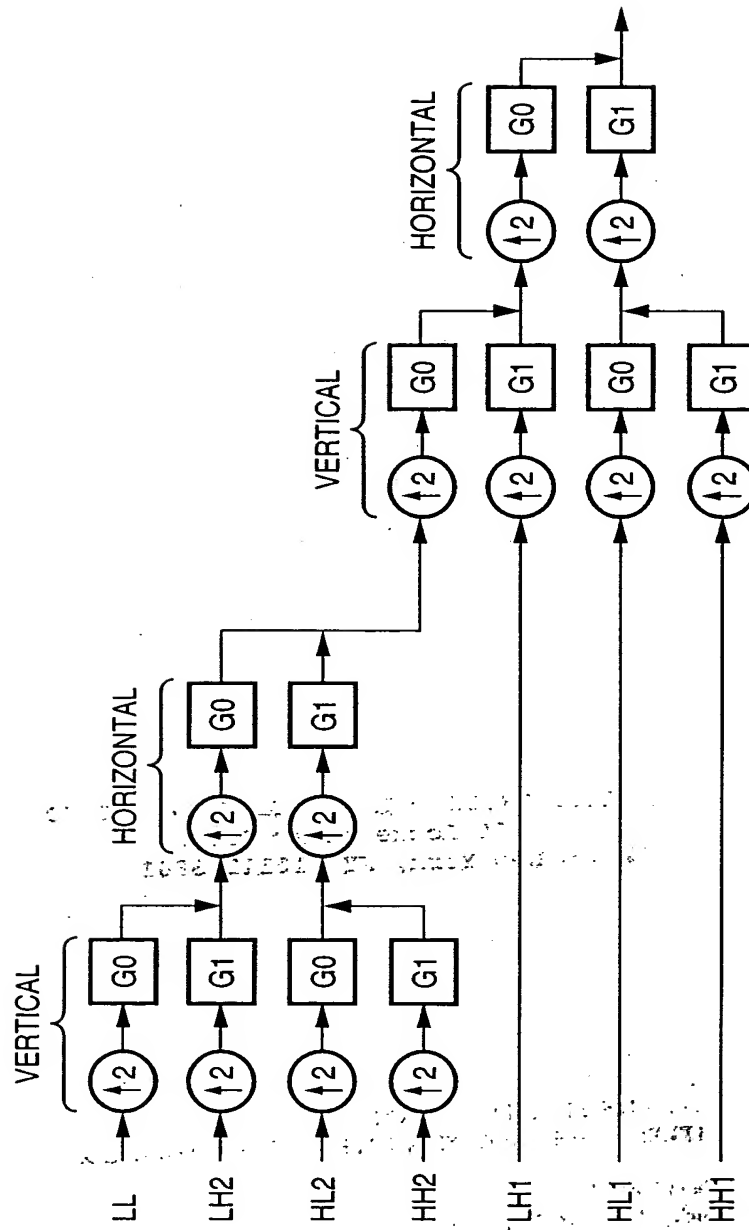
91ST TO 120TH FRAMES

FIG. 6F

END OF SWITCHING

FIG. 7



**FIG. 8**

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FIG. 9

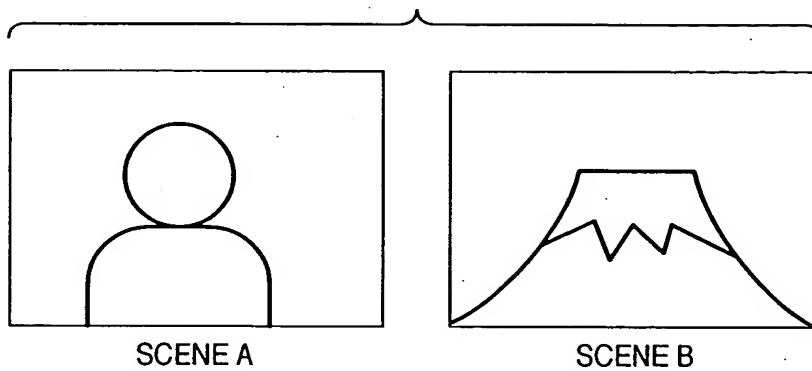


FIG. 9 is a schematic diagram of a system for processing video data. The system includes a video input device 10, a video processing unit 20, and a video output device 30. The video input device 10 is connected to the video processing unit 20, which is in turn connected to the video output device 30. The video processing unit 20 is configured to receive video data from the video input device 10, process the video data, and output the processed video data to the video output device 30. The video processing unit 20 may include a video decoder, a video processor, and a video encoder. The video input device 10 may be a camera, a video camera, or a video capture device. The video output device 30 may be a monitor, a video display, or a video storage device.

FIG. 10 is a schematic diagram of a system for processing video data. The system includes a video input device 10, a video processing unit 20, and a video output device 30. The video input device 10 is connected to the video processing unit 20, which is in turn connected to the video output device 30. The video processing unit 20 is configured to receive video data from the video input device 10, process the video data, and output the processed video data to the video output device 30. The video processing unit 20 may include a video decoder, a video processor, and a video encoder. The video input device 10 may be a camera, a video camera, or a video capture device. The video output device 30 may be a monitor, a video display, or a video storage device.

FIG. 10

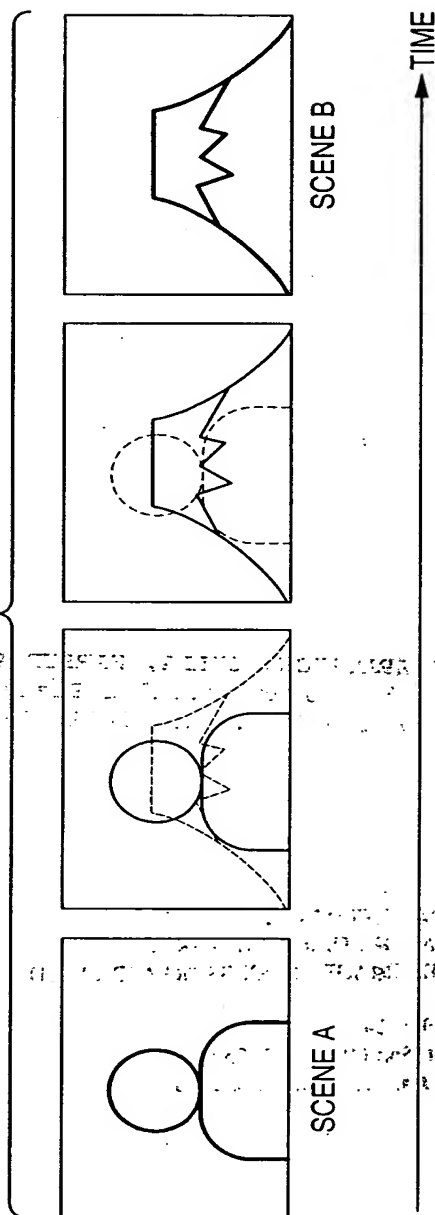
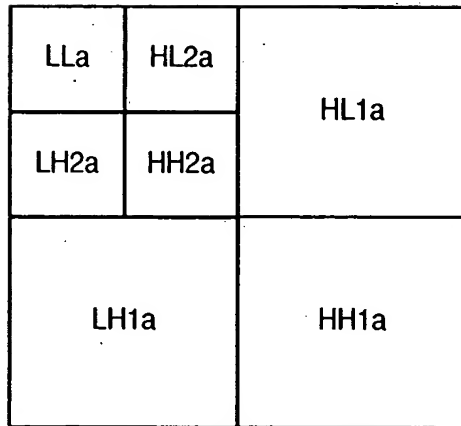
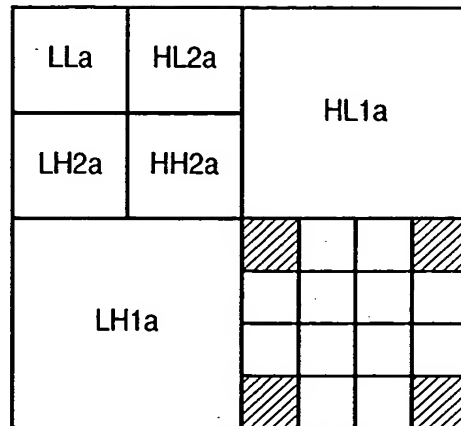
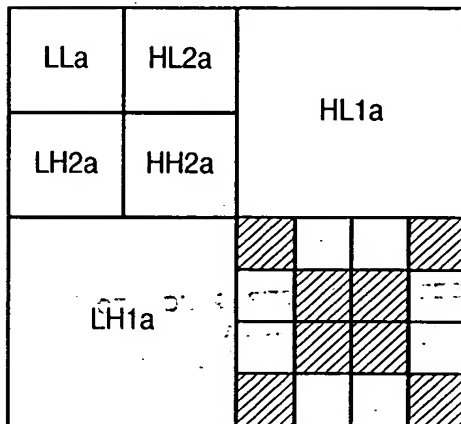


FIG. 11A

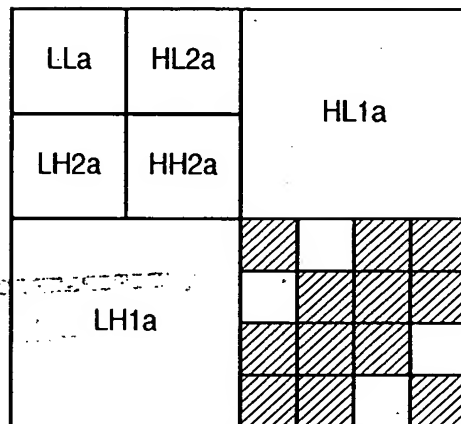
START OF SWITCHING

FIG. 11B

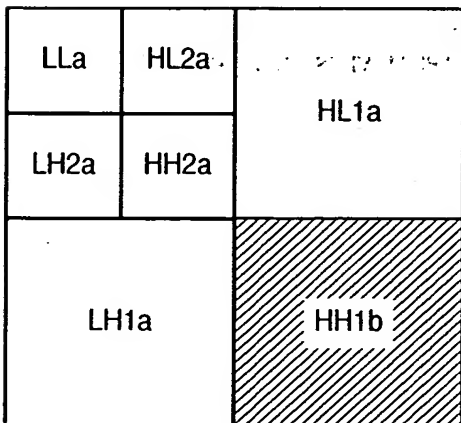
1ST TO 8TH FRAMES

FIG. 11C

9TH TO 16TH FRAMES

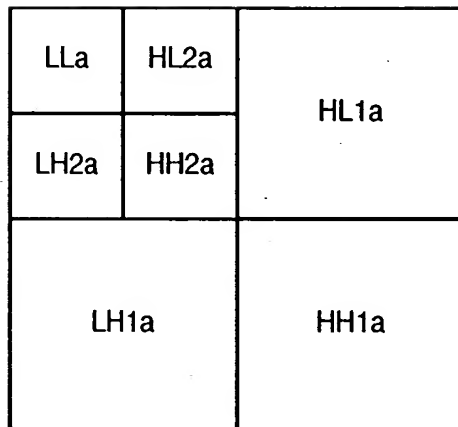
FIG. 11D

17TH TO 24TH FRAMES

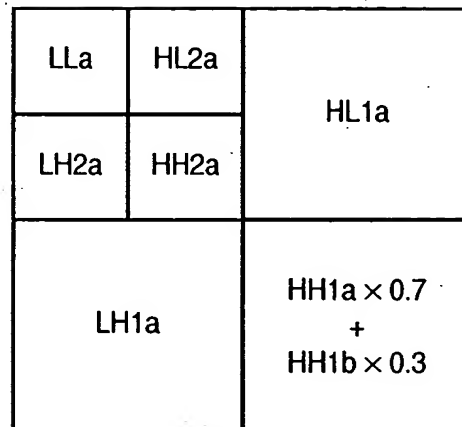
FIG. 11E

25TH TO 32ND FRAMES

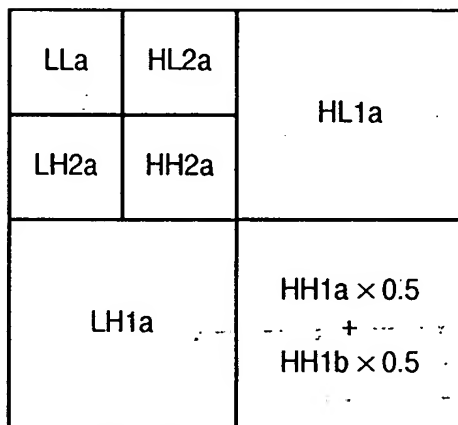


FIG. 12A

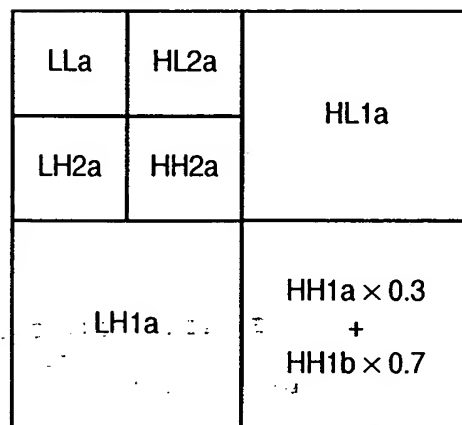
START OF SWITCHING

FIG. 12B

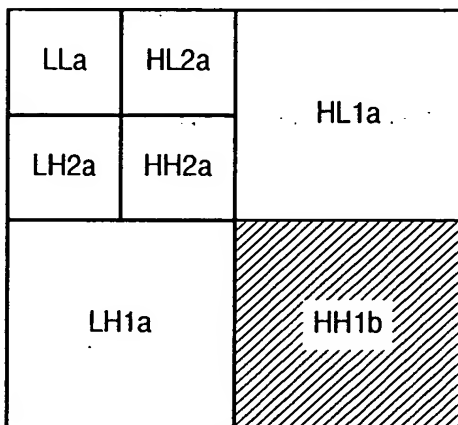
1ST TO 8TH FRAMES

FIG. 12C

9TH TO 16TH FRAMES

FIG. 12D

17TH TO 24TH FRAMES

FIG. 12E

25TH TO 32ND FRAMES

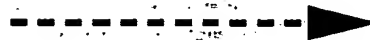


FIG. 13

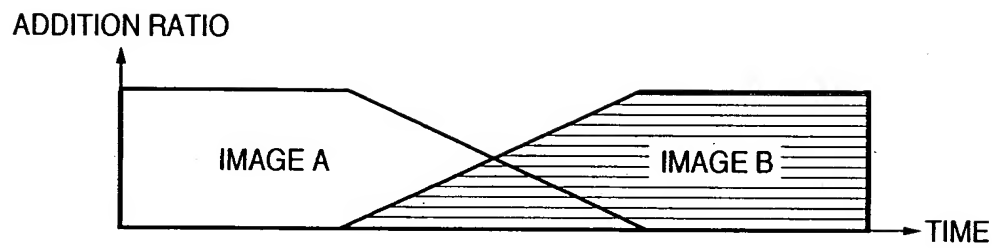


FIG. 14

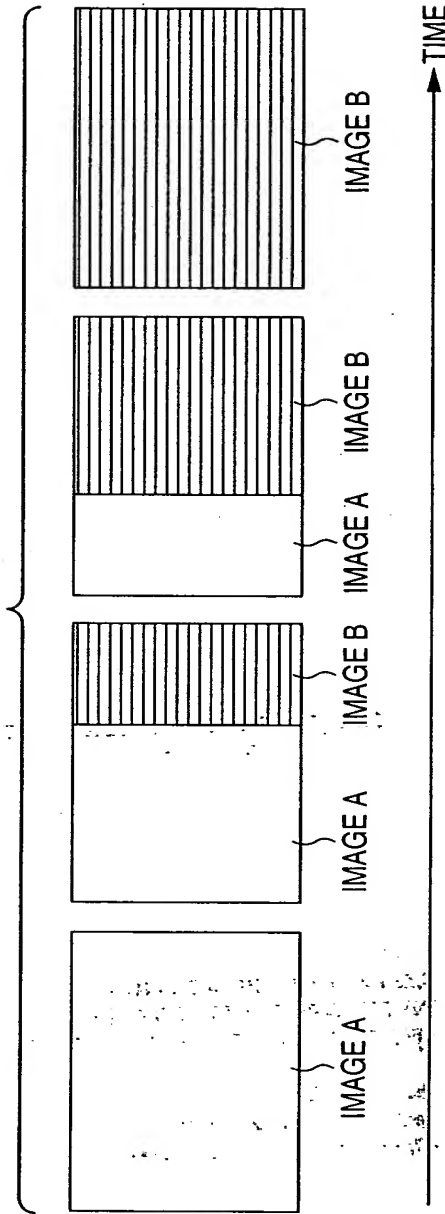


FIG. 15

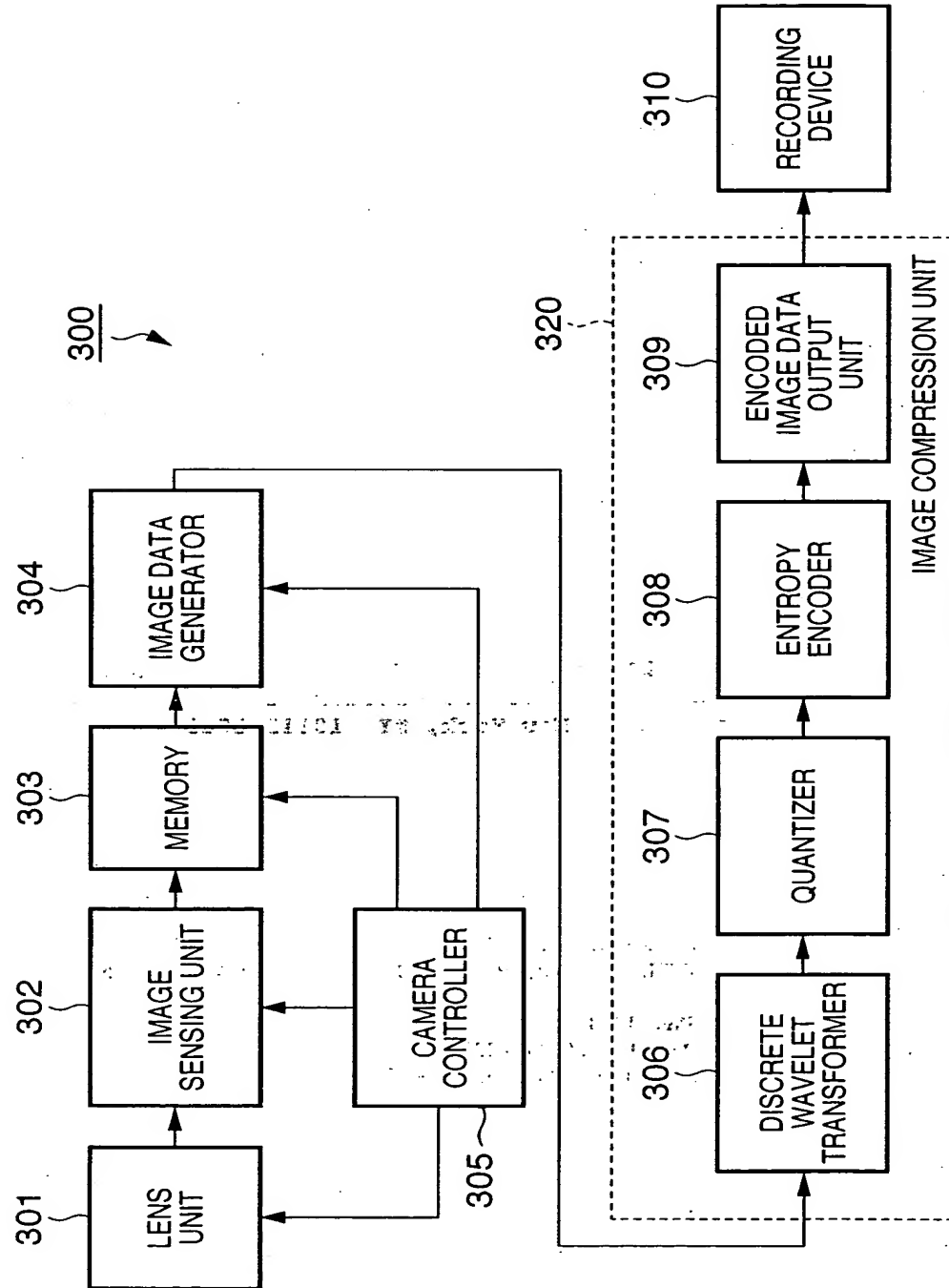


FIG. 16

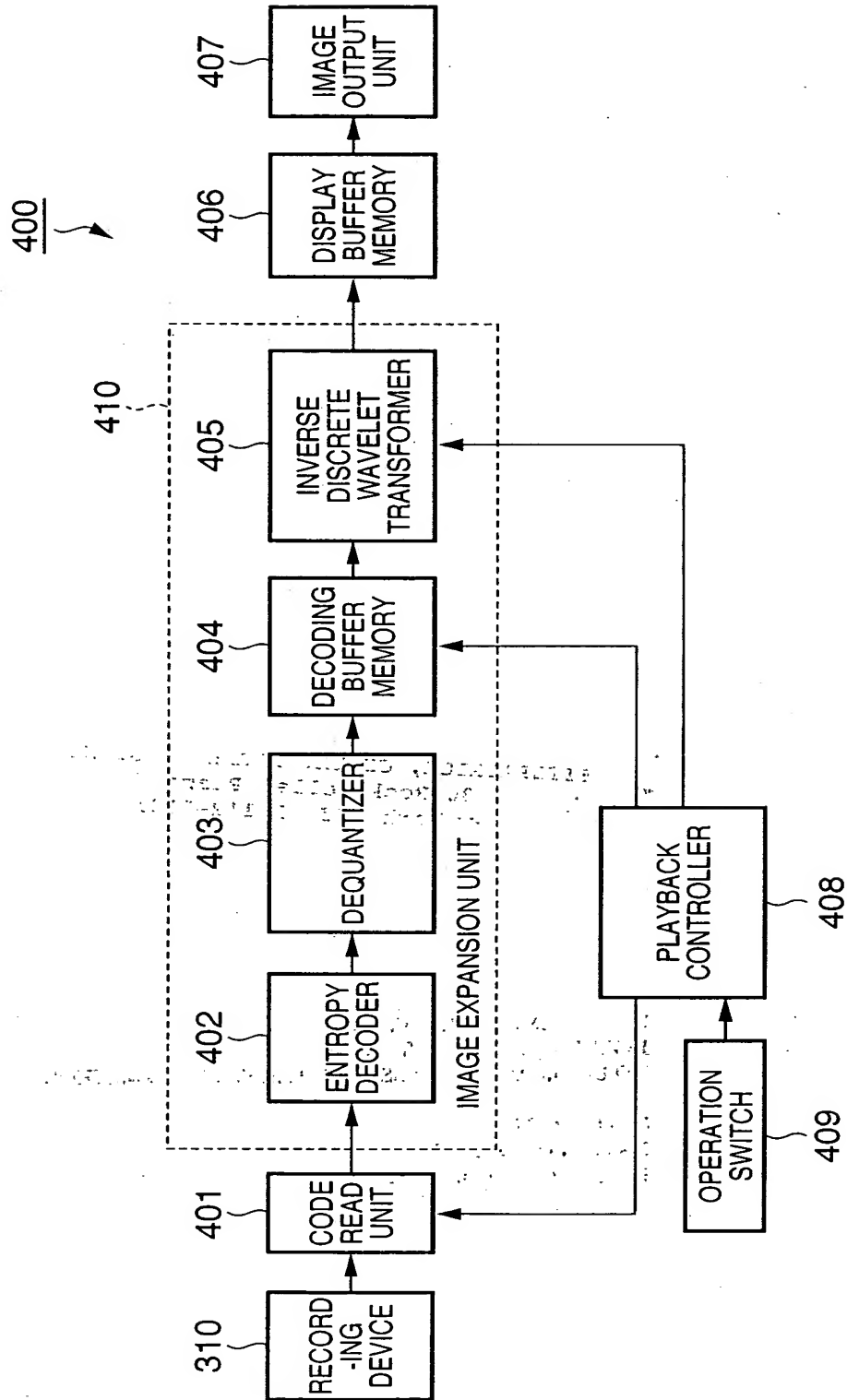
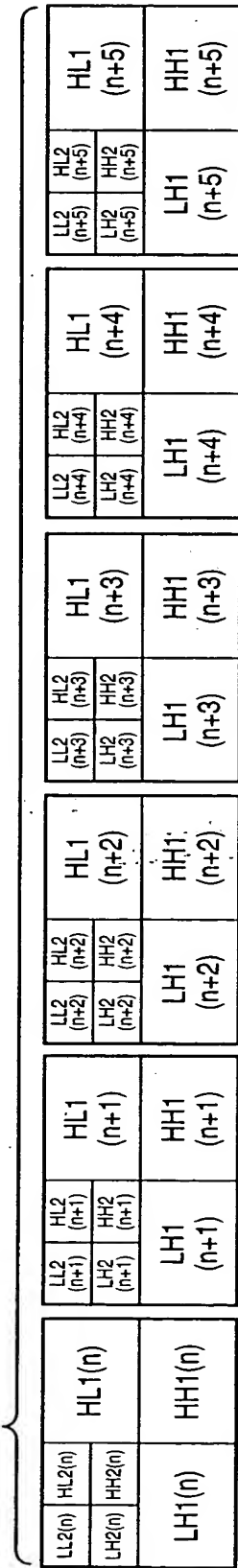


FIG. 17A



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FIG. 17B

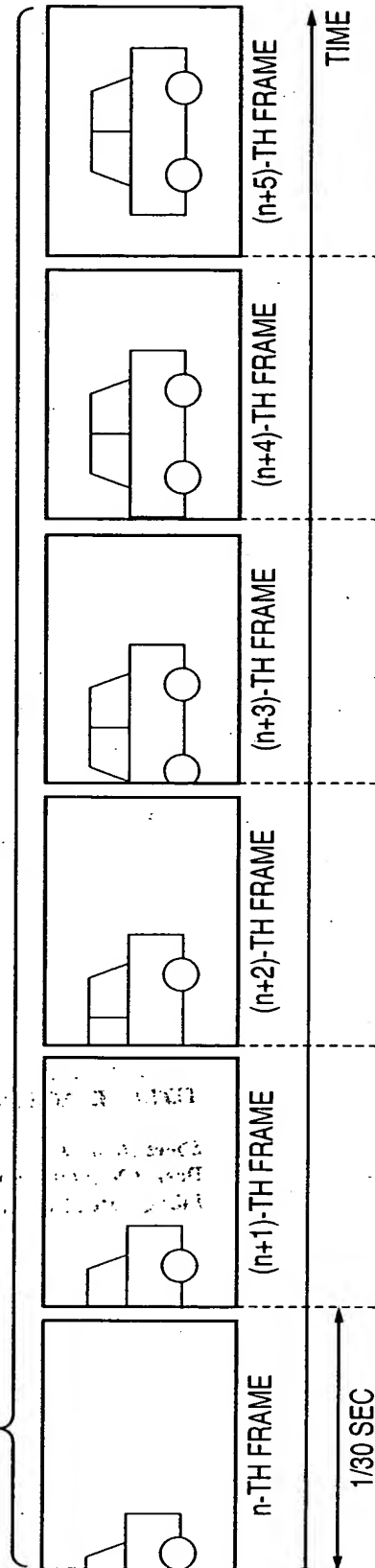
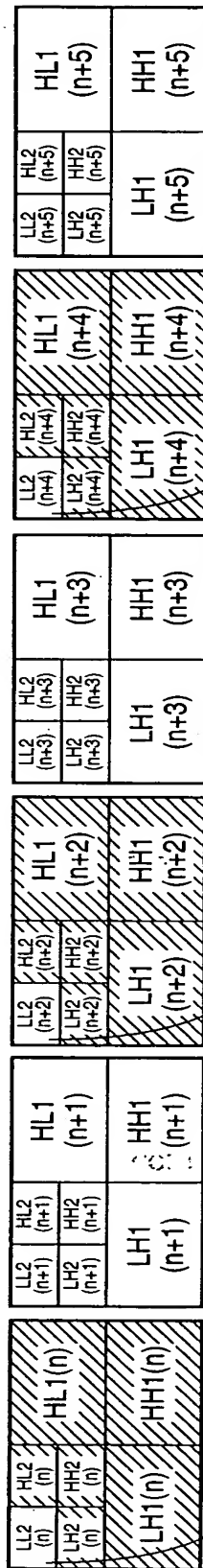


FIG. 18A



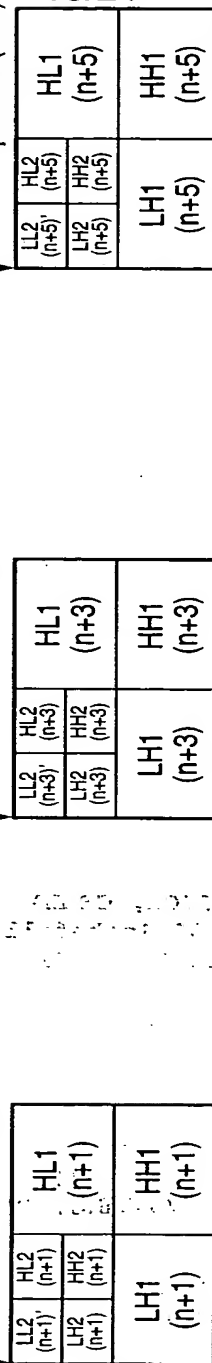
$$\text{WEIGHTED MEAN } LL2(n+5)' = \alpha \times LL2(n+5) + \beta \times LL2(n+4)$$

$$\text{WEIGHTED MEAN } LL2(n+3)' = \alpha \times LL2(n+3) + \beta \times LL2(n+2)$$

$$\text{WEIGHTED MEAN } LL2(n+1)' = \alpha \times LL2(n+1) + \beta \times LL2(n)$$

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FIG. 18B



DECODE

DECODE

DECODE

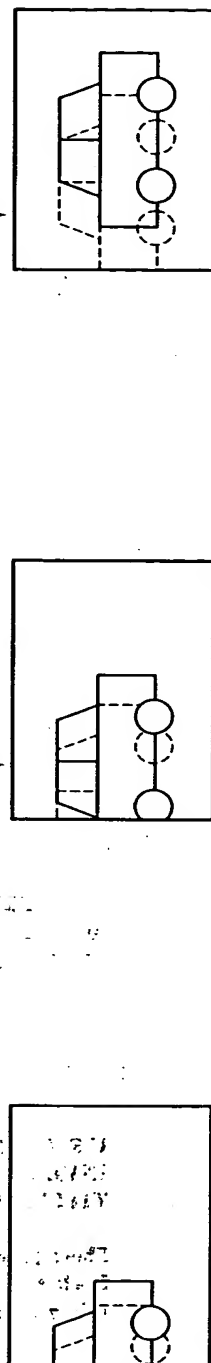


FIG. 18C

(n+5)-TH FRAME

(n+3)-TH FRAME

(n+1)-TH FRAME

TIME

1/30 SEC

FIG. 19A

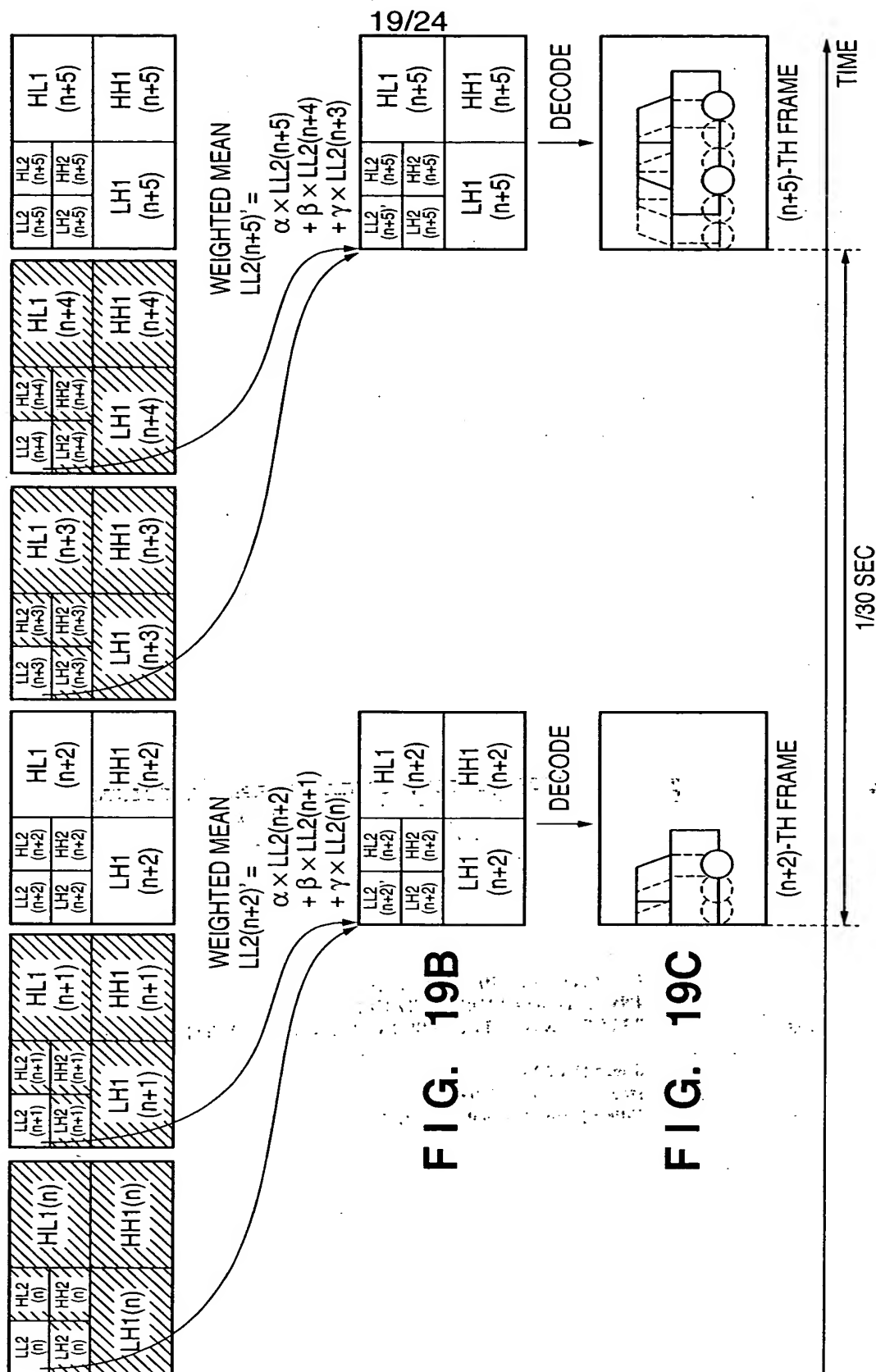


FIG. 20A

LL2(n)	HL2(n)	HL1(n)
LH2(n)	HH2(n)	
LH1(n)	HH1(n)	

LL2(n+1)	HL2(n+1)	HL1(n+1)
LH2(n+1)	HH2(n+1)	
LH1(n+1)		HH1(n+1)

WEIGHTED MEAN

$$\begin{aligned}
 &\rightarrow LL2(n+1)' = \alpha \times LL2(n+1) + \beta \times LL2(n) \\
 &\rightarrow HL2(n+1)' = \alpha \times HL2(n+1) + \beta \times HL2(n) \\
 &\rightarrow LH2(n+1)' = \alpha \times LH2(n+1) + \beta \times LH2(n) \\
 &\rightarrow HH2(n+1)' = \alpha \times HH2(n+1) + \beta \times HH2(n)
 \end{aligned}$$

FIG. 20B

LL2(n+1)'	HL2(n+1)'	HL1(n+1)
LH2(n+1)'	HH2(n+1)'	
LH1(n+1)		HH1(n+1)

FIG. 21A

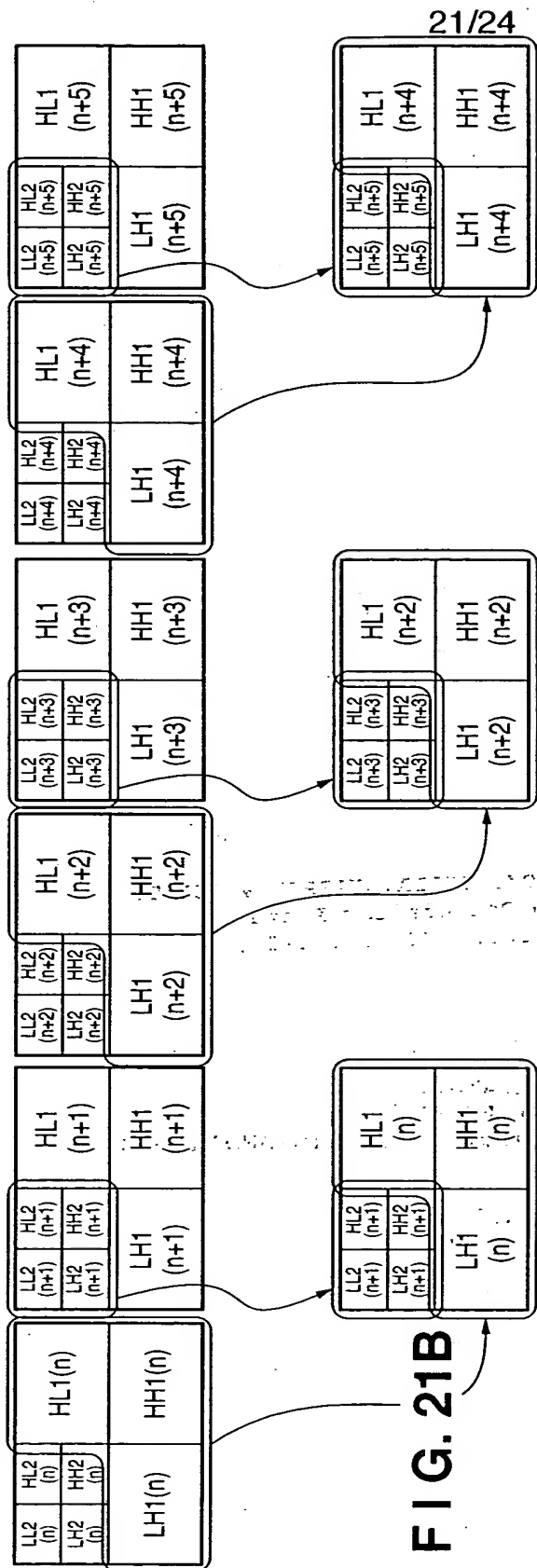


FIG. 21B

DECODE

DECODE

DECODE

FIG. 21C

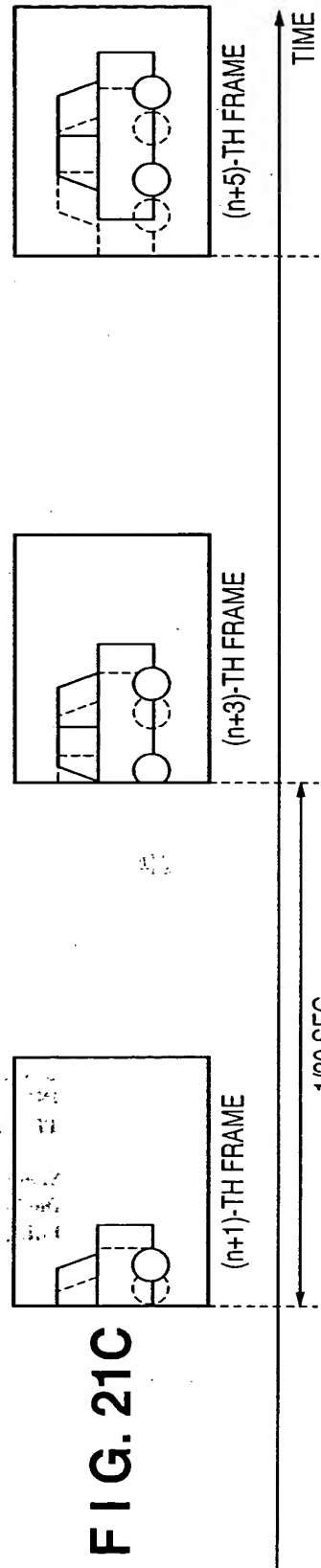


FIG. 23

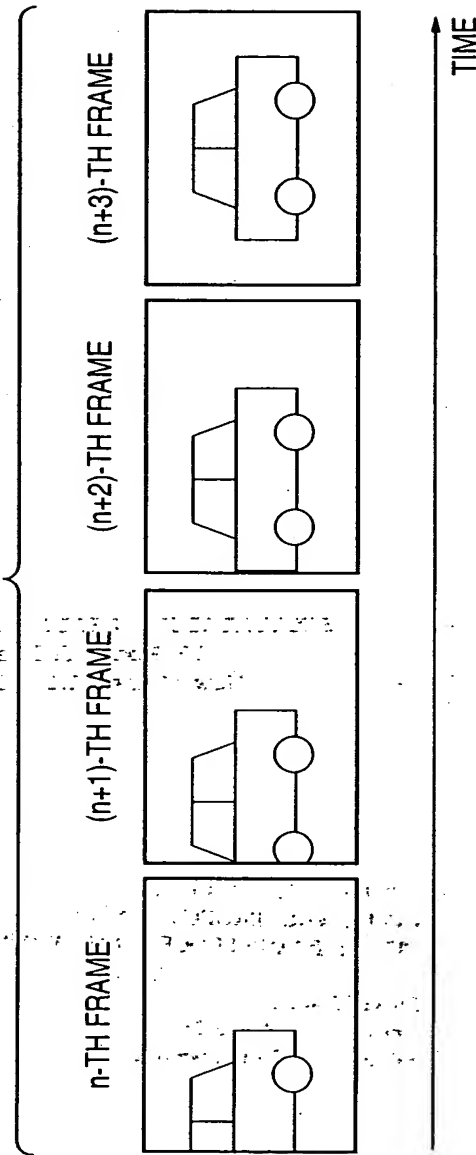


FIG. 24

